IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	§	
MOK, et al.	§	
	§	Group Art Unit: 2818
Serial No.: 10/823,849	§	
	§	
Confirmation No.: 5507	§	
	§	Examiner: David Vu
Filed: April 13, 2004	§	
	§	
For: TWO PISITION ANNEAL CHAMBER	§	

MAIL STOP: APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

APPEAL BRIEF

Applicants submit this Appeal Brief to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner of Group Art Unit 2818 dated March 3, 2006, finally rejecting claims 1-21 and 26-29. The final rejection of claims 1-21 and 26-29 is appealed. This Appeal Brief is believed to be timely since mailed by the due date of July 31, 2006, as set by mailing a Notice of Appeal on May 30, 2006. Authorization to charge the fee of $500.00 for filing this brief is provided on a separate fee transmittal. Please charge any additional fees that may be required to make this Appeal Brief timely and acceptable to Deposit Account No. 20-0782/APPM/008298/KMT.

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Real Party in Interest

The present application has been assigned to Applied Materials, Inc., 3050 Bowers Avenue, Santa Clara, California 95054.

Related Appeals and Interferences

Appellant asserts that no other appeals or interferences are known to the Appellant, the Appellant's legal representative, or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1-21 and 26-29 are pending in the application. Claims 1-25 were originally presented in the application. Claims 22-25 were cancelled without prejudice and claims 26-29 were added in the response to the Restriction Requirement dated June 15, 2005.

Claims 1-21 and 26-29 stand finally rejected as discussed below. The final rejection of claims 1-21 and 26-29 is appealed.

Status of Amendments

All claim amendments have been entered by the Examiner and are included in the Claims Appendix.

Summary of Claimed Subject Matter

Claimed embodiments of the invention provide an annealing apparatus and method for a semiconductor processing platform. The annealing apparatus includes a plurality of isolated annealing chambers. Each of the annealing chambers has a heating plate positioned in a sealed processing volume, a cooling plate positioned in the processing volume, and a substrate transfer mechanism positioned in the processing volume and configured to transfer substrates between the heating plate and the cooling plate. The annealing system further includes a gas supply source selectively in communication with each of the individual annealing chamber. (*See*, Abstract and Summary)

In the embodiments of independent claim 1, an annealing system for a semiconductor processing platform is provided, comprising a plurality of isolated annealing chambers (Figures 1 and 3, paragraph 23), each of the isolated annealing chambers comprising a heating plate positioned in an enclosed processing volume and configured to support a substrate thereon in a substantially face up orientation (paragraphs 23, 28, and 32, and Figures 6 and 7), a cooling plate positioned in the enclosed processing volume and configured to support a substrate thereon in a substantially face up orientation (paragraphs 12, 23, 28, and 31), and a substrate transfer mechanism positioned in the processing volume and configured to transfer substrates between the heating plate and the cooling plate (paragraph 35).

In the embodiments of independent claim 11, an annealing station for a semiconductor processing system is provided, comprising a plurality of individual annealing chambers, each annealing chamber defining an isolated processing volume (Figures 1 and 3, paragraph 23), a heating plate positioned in the processing volume (paragraphs 23, 28, and 32, and Figures 6 and 7), a cooling plate positioned in the processing volume (paragraphs 12, 23, 28, and 31), and a substrate transfer robot positioned to receive a substrate from an externally positioned robot in a face up orientation and position the substrate onto the heating plate and the cooling plate in the face up orientation (paragraph 35).

In the embodiments of independent claim 26, a semiconductor processing platform is provided, comprising a substrate loading station (Figures 1 and 3, paragraph 23), at least one substrate plating cell positioned in communication with the loading station (Figures 1 and 3, paragraph 23), at least one substrate cleaning cell positioned in communication with the loading station (Figures 1 and 3, paragraph 23), and an annealing station positioned in communication with the loading station, the annealing station comprising a plurality of annealing chambers (Figures 1 and 3, paragraph 23), each of the annealing chambers comprising an enclosure forming a sealed processing volume (Figures 1 and 3, paragraph 23), a heating plate positioned in the sealed processing volume of each of the annealing chambers (paragraphs 23, 28, and 32, and Figures 6 and 7), a cooling plate positioned in the sealed processing volume of each of the annealing chambers (paragraphs 12, 23, 28, and 31), and a substrate transfer mechanism positioned to transfer substrates between the heating plate and the cooling plate (paragraph 35).

Grounds of Rejection to be Reviewed on Appeal

1. Claims 1-21 and 26-29 stand rejected under 35 U.S.C. § 102(e), as being anticipated by *Yang et al.* (US 2004/0016637).

ARGUMENTS

A. Rejection of Claims 1-21 and 26-29 over *Yang et al.*

Claims 1-21 and 26-29 stand rejected under 35 U.S.C. § 102(e), as being anticipated by or obvious in view of *Yang et al.* (U.S. Patent Application Publication No. 2004/0016637; serial number 10/616,284). The Examiner states that the effective filing date of *Yang et al.* is July 24, 2002, the filing date of a provisional application 60/398,345. Applicants have respectfully traversed the rejections on grounds that the claimed subject matter of the instant application has an effective filing date prior to the effective filing date of the subject matter relied on in *Yang et al.*

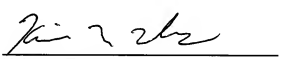
Applicants respectfully submit that the Examiner erroneously relies on disclosure of an annealing system in *Yang et al.* because the disclosed annealing system is not disclosed in the priority applications (serial numbers 10/268,284 and 60/398,345) of *Yang et al.*, and is only disclosed in *Yang et al.* (serial number 10/616,284) as of its filing date of July 8, 2003. The two parent applications (serial numbers 10/268,284 and 60/398,345) of *Yang et al.* do not teach, show, or suggest an annealing system. Thus, the relevant reference date of the subject matter relied on in *Yang et al.* is its filing date of July 8, 2003.

The instant application claims priority to United States provisional patent application serial number 60/463,860, and the claims on appeal are entitled to the filing date of April 18, 2003. Therefore, the relevant invention date of the instant invention of April 18, 2003 is earlier than the relevant reference date of July 8, 2003 for the relied and disclosed subject matter of *Yang et al.* Accordingly, withdrawal of the rejection based on *Yang et al.* and allowance of claims 1-21 and 26-29 are respectively requested.

CONCLUSION

The Examiner erroneously rejected claims 1-21 and 26-29 under 35 U.S.C. § 102 (e) over *Yang et al.* because the effective filing date is July 8, 2003, which is later than the effective filing date of the instant invention of April 18, 2003. Therefore, it is believed that the rejection made by the Examiner should be reversed. Thus, Applicants respectfully request reversal of the rejection and allowance of claims 1-21 and 26-29.

Respectfully submitted,



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APPENDIX OF PENDING CLAIMS

1. (Original) An annealing system for a semiconductor processing platform, comprising a plurality of isolated annealing chambers, each of the isolated annealing chambers comprising:

a heating plate positioned in an enclosed processing volume and configured to support a substrate thereon in a substantially face up orientation;

a cooling plate positioned in the enclosed processing volume and configured to support a substrate thereon in a substantially face up orientation; and

a substrate transfer mechanism positioned in the processing volume and configured to transfer substrates between the heating plate and the cooling plate.

2. (Original) The annealing system of claim 1, wherein the heating plate comprises a substantially planar upper substrate receiving surface having at least one vacuum chucking aperture formed therein.

3. (Original) The annealing chamber of claim 2, wherein the heating plate comprises at least one of a resistive heating element and an inductive heating element positioned in an interior portion of the heating plate below the substrate receiving surface.

4. (Original) The annealing system of claim 1, wherein the cooling plate comprises a substrate support member having at least one of a liquid cooling channel formed into an interior portion thereof and a thermoelectric cooling device positioned in an interior portion thereof.

5. (Original) The annealing system of claim 1, wherein the cooling plate comprises at least one vacuum aperture formed into an upper surface thereof.

6. (Original) The annealing system of claim 1, wherein the substrate transfer mechanism comprises a pivotally actuated robot arm having a distal substrate supporting blade positioned thereon.

7. (Original) The annealing system of claim 6, wherein the substrate support blade further comprises a plurality of inwardly facing substrate support tabs positioned below a main upper body portion of the support blade, the support tabs being positioned to support the substrate via contact with a backside of the substrate.

8. (Previously Presented) The annealing system of claim 7, wherein the heating plate and the cooling plate have a plurality of notches formed into a perimeter thereof, the plurality of notches being configured to receive the plurality of inwardly facing substrate support tabs when the robot blade is lowered toward the heating and cooling plates.

9. (Original) The annealing chamber of claim 1, wherein the plurality of isolated annealing chambers further comprise at least 3 stacked annealing chambers, each of the at least three stacked annealing chambers being fluidly separated from each other.

10. (Original) The annealing chamber of claim 1, further comprising a gas source in fluid communication with an interior volume of each of the annealing chambers, the gas source being configured to supply an inert gas to the processing volumes to maintain the oxygen content below about 100 ppm.

11. (Original) An annealing station for a semiconductor processing system, comprising:

a plurality of individual annealing chambers, each annealing chamber defining an isolated processing volume;

a heating plate positioned in the processing volume;

a cooling plate positioned in the processing volume; and

a substrate transfer robot positioned to receive a substrate from an externally positioned robot in a face up orientation and position the substrate onto the heating plate and the cooling plate in the face up orientation.

12. (Original) The annealing station of claim 11, wherein the individual processing volumes are fluidly isolated from each other.

13. (Original) The annealing station of claim 11, wherein the substrate transfer robot comprises:

a pivotally and vertically actuatable arm member; and

a blade member attached to a distal end of the arm member, the blade member having a plurality of inwardly extending substrate support tabs positioned thereon that are configured to engage a backside of a substrate.

14. (Previously Presented) The annealing station of claim 13, wherein the heating plate and the cooling plate have a plurality of vertically oriented channels formed into a perimeter of the plates, wherein the vertically oriented channels are configured to receive the inwardly extending substrate support tabs with the blade is lowered to the plane of the plates.

15. (Previously Presented) The annealing station of claim 11, wherein at least one of the heating plate and the cooling plate has a vacuum aperture formed into an upper substrate supporting surface, the vacuum aperture being configured to chuck a backside of the substrate to the respective plate.

16. (Previously Presented) The annealing station of claim 11, wherein a fluid channel is formed into an outer body portion of each of the plurality of individual annealing chambers, the fluid channel being in fluid communication with a cooling fluid source.

17. (Previously Presented) The annealing station of claim 11, wherein the heating plate is configured to heat a non-production surface of the substrate positioned thereon.

18. (Previously Presented) The annealing station of claim 11, further comprising a resistive heating element positioned in an interior portion of the heating plate.

19. (Previously Presented) The annealing station of claim 11, further comprising a sealable access door positioned in an outer body portion of the chamber.

20. (Previously Presented) The annealing station of claim 11, further comprising a vacuum source individually in communication with each of the processing volumes, the vacuum source being configured to generate a reduced pressure in each of the processing volumes.

21. (Previously Presented) The annealing station of claim 11, further comprising a processing gas supply selectively in communication with each of the annealing chambers.

22 – 25. (Cancelled).

26. (Previously Presented) A semiconductor processing platform, comprising:
a substrate loading station;

at least one substrate plating cell positioned in communication with the loading station;

at least one substrate cleaning cell positioned in communication with the loading station; and

an annealing station positioned in communication with the loading station, the annealing station comprising a plurality of annealing chambers, each of the annealing chambers comprising:

an enclosure forming a sealed processing volume;

a heating plate positioned in the sealed processing volume of each of the annealing chambers;

a cooling plate positioned in the sealed processing volume of each of the annealing chambers; and

a substrate transfer mechanism positioned to transfer substrates between the heating plate and the cooling plate.

27. (Previously Presented) The semiconductor processing platform of claim 26, further comprising at least one gas supply source selectively in communication with each of the sealed processing volumes, and adapted to supply a processing gas to each of the sealed processing volumes.

28. (Previously Presented) The semiconductor processing platform of claim 26, further comprising at least one vacuum source individually in communication with each of the sealed processing volumes, the vacuum source being configured to generate a reduced pressure individually in each of the processing volumes.

29. (Previously Presented) The semiconductor processing platform of claim 26, wherein the plurality of the annealing chambers are positioned in vertically stacked configuration.

EVIDENCE APPENDIX

No evidence is submitted.

RELATED PROCEEDINGS APPENDIX

No copies of decisions rendered by a court or the Board in the related appeal or interference listed on page 4 of this Brief are included as there have been no related appeal or interference listed on page 4 of this Brief.